

THAT WHICH IS CLAIMED IS:

1. A labeled semiconductor material comprising:
a surface of a semiconductor material; and
a first metal layer on portions but not all of said surface;
5 said metal layer forming a pattern with rotational symmetry of C_n , where n is at least
2.
2. A labeled semiconductor according to Claim 1 and further comprising:
a second metal layer on portions but not all of said surface of said semiconductor
10 material;
 said second metal layer forming a pattern different from said first metal layer pattern;
 and
 said second pattern having rotational symmetry of C_n where n is at least 2.
- 15 3. A labeled semiconductor according to Claim 2 wherein portions of said second
 metal layer overlie portions of said first metal layer.
- 20 4. A labeled semiconductor according to Claim 2 wherein each of said first and
 second patterns forms an X pattern.
- 25 5. A labeled semiconductor according to Claim 4 wherein each X pattern further
 comprises a tab portion perpendicular to at least one of the arms of said X pattern.
6. A labeled semiconductor according to Claim 1 wherein said C_n pattern includes
25 linearly sequential metallized and non-metallized portions.
7. A labeled semiconductor according to Claim 2 wherein said first and second metal
 layers comprise concentric circles.

8. A labeled semiconductor according to Claim 1 wherein said metal layers form an ohmic contact to said semiconductor material.

9. A labeled semiconductor material according to Claim 8 comprising silicon 5 carbide.

10. A labeled semiconductor material according to Claim 9 wherein said metal layer is selected from the group consisting of nickel, titanium, gold, platinum, vanadium, aluminum, alloys thereof and layered combinations thereof.

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11. A semiconductor structure comprising:
a substrate having at least one planar face;
a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and
15 a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern.

12. A semiconductor structure according to Claim 11 wherein portions of said second metal layer overlie portions of said first metal layer.

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13. A semiconductor structure according to Claim 11 further comprising a epitaxial layer on the opposite side of said substrate from said planar face and said metal layers.

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14. A semiconductor structure according to Claim 13 wherein said substrate and said

epitaxial layer comprise a semiconductor device.

15. A semiconductor structure according to Claim 14 wherein said device is selected from the group consisting of junction diodes, bipolar transistors, thyristors, MESFETS, JFETS, MOSFETS and photodetectors.

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16. A semiconductor structure according to Claim 14 wherein said metal layers form an ohmic contact to said device.

17. A semiconductor structure according to Claim 16 wherein said substrate and said 5 epitaxial layer are silicon carbide and said metal layers are selected from the group consisting of nickel, titanium, gold, alloys thereof, and layered combinations thereof.

18. A semiconductor structure according to Claim 11 wherein said first and second geometric patterns have C_n rotational symmetry where n is at least 2.

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19. A semiconductor device according to Claim 14 wherein said device comprises a light emitting diode or laser diode that includes a p-n junction, and with said ohmic contact comprising a layer of nickel on said substrate and a layer selected from the group consisting of titanium-gold alloys and titanium-platinum-gold alloys on said nickel layer.

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20. A semiconductor wafer comprising:

respective primary and secondary orthogonal flats;

respective front and back planar faces;

a plurality of devices on said wafer;

20 each said device having a first metal layer on said planar face, and covering some, but not all of said planar face in a first predetermined geometric pattern; and

each said device having a second metal layer on said planar face, and covering some, but not all of said planar face in a second geometric pattern that is different from said first geometric pattern.

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21. A semiconductor wafer according to Claim 20 wherein the devices on said wafer are identical to one another.

30 22. A semiconductor wafer according to Claim 20 wherein said devices are aligned in a predetermined relationship with said flats.

23. A semiconductor wafer according to Claim 20 wherein said first and second patterns have C_n rotational symmetry where n is at least 2.

24. A semiconductor wafer according to Claim 20 wherein said wafer comprises a silicon carbide substrate and at least one silicon carbide epitaxial layer.

25. A semiconductor wafer according to Claim 20 wherein said metal layers form respective ohmic contacts to said devices.

10 26. A semiconductor wafer according to Claim 20 wherein said devices are selected from the group consisting of: junction diodes, bipolar transistors, thyristors, MESFETS, JFETS, MOSFETS and photodetectors.

15 27. A semiconductor wafer according to Claim 20 wherein:
said wafer comprises a silicon carbide substrate and at least one silicon carbide epitaxial layer;
said devices comprise light emitting diodes or laser diodes that include a p-n junction;
and
said metal layers comprise a layer of nickel on said substrate and a layer of a 20 titanium-gold alloy on said nickel layer that form respective ohmic contacts to said devices.

25 28. A quality control method for manufacturing a semiconductor device comprising:
placing a first metal layer on a semiconductor face of a device in a first predetermined pattern; and
placing a second metal layer on the same face of the device as the first layer and in a second predetermined geometric pattern that is different from the first pattern.

29. A semiconductor manufacturing method according to Claim 28 and further comprising:

inspecting the device to identify the presence or absence of one or both of the patterns on the face.

30. A quality control manufacturing method according to Claim 29 and further
5 comprising discarding the device when one or both of the predetermined patterns are absent.

31. A quality control manufacturing method according to Claim 29 wherein the step of inspecting the face of the device comprises illuminating the metallized face and scanning the metallized face with a machine inspection system.

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32. A quality control method according to Claim 29 wherein the step of inspecting the device comprises inspecting a transparent device by illuminating the face opposite from the metal layers and scanning the opposite face with a machine inspection system.

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33. A quality control method according to Claim 29 wherein:
the step of placing the metal layers comprises placing a pattern with rotational symmetry of C_n , where n is at least 2; and
the step of inspecting each device comprises inspecting either face of the device to identify the presence or absence of the C_n pattern.

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34. A quality control method for manufacturing wafers with a plurality of semiconductor devices thereon, the method comprising:

placing a first metal layer in a first predetermined geometric pattern on a semiconductor face of each device; and

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placing a second metal layer on the same face of each device as said first layer and in a second predetermined geometric pattern that is different from said first geometric pattern;
inspecting the face of each device to identify the presence or absence of one or both of the patterns on each device; and

discarding the devices for which one or both of the patterns are absent.

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35. A quality control method according to Claim 8 wherein the step of inspecting the face of each device comprises evaluating each device with a machine inspection system.

36. A quality control method according to Claim 34 wherein:
5 the step of placing the metal layers comprises placing a pattern with rotational symmetry of C_n , where n is at least 2; and
the step of inspecting each device comprises inspecting either face of the device to identify the presence or absence of the C_n pattern.

10 37. A quality control method according to Claim 34 comprising forming the semiconductor devices on the wafer prior to the step of placing the first metal layer on the devices.

15 38. A quality control method according to Claim 37 wherein the step of forming the semiconductor devices comprises forming at least one epitaxial layer on a substrate wafer.

39. A quality control method according to Claim 38 comprising forming an epitaxial layer of silicon carbide on a silicon carbide substrate.

20 40. A quality control method according to Claim 39 comprising placing the metal layers on the face of the substrate opposite the epitaxial layer.

41. A quality control method according to Claim 34 comprising:
placing the metal layers on a wafer that includes at least one flat; and
25 aligning the metal layers with the flat in a predetermined relationship.

42. A quality control method according to Claim 41 wherein the step of inspecting the devices comprises aligning the flat of the wafer with a machine inspection system and thereafter evaluating each device with the machine inspection system.

43. A quality control method according to Claim 35 wherein the step of inspecting the devices comprises inspecting a transparent device by illuminating the face of the wafer opposite from the metal layers and scanning the illuminated face with a machine inspection system.

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